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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/005,794	11/02/2001	Mark Brooks	201028	1406

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EXAMINER	
GLENN, KIMBERLY E	
ART UNIT	PAPER NUMBER
2817	

DATE MAILED: 01/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/005,794	BROOKS ET AL.	
	Examiner	Art Unit	
	Kimberly E Glenn	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 5/19/03.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-20 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the plurality of apertures must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 4, 6, 8 and 15- 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Talisa et al US Patent 5,974,335. (Of record)

Talisa et al disclose a delay line comprising a tapered delay line (68a 68b 68c 68d), a dielectric substrate 54 and a ground plane 66. The patterned delay line has a predefined length and a predefined line width from transformer 26 to transformer 27. Figure 1a show each transformer, each having a tapered line width having a wide portion W, matching that of the deposited delay line and which tapers down to a narrow portion N, which is connected to a signal input or output. Input 15 and output 20 of each spiral line segment can be provided with coplanar

line transition input and output pad pairs 22a, 22b and 24a, 24b, respectively. (Figures 1, 1a, 2 and 3)

With regard to claim 3, the limitation concerning the signal conductor and ground layers being sputtered onto a ceramic substrate will not be given any patentable weight. The independent claim discloses an apparatus and the patentability of the claims are based on the apparatus not a method of making the apparatus.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 11, 12 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Talisa et al US Patent 5,974,335 in view of Sasaki et al US Patent 6,346,863 (both of record).

The primary reference, Talisa et al teaches a delay line comprising a tapered delay line (68a 68b 68c 68d), a dielectric substrate 54 and a ground plane 66. The patterned delay line has a predefined length and a predefined line width from transformer 26 to transformer 27. Figure 1a show each transformer, each having a tapered line width having a wide portion W, matching that of the deposited delay line and which tapers down to a narrow portion N, which is connected to a signal input or output. Input 15 and output 20 of each spiral line segment can be provided with coplanar line transition input and output pad pairs 22a, 22b and 24a, 24b, respectively. (Figures 1, 1a, 2 and 3)

Thus, Talisa et al is shown to teach all the limitation of the claim with the exception of the spacing of the unbounded pathway portion to an adjoining one the plurality of pathway portions is less than the spacing between the others of the plurality of pathway portion.

Sasaki et al teaches a circuit comprising a signal layer (microstriplines 21 and 22) including at least one signal conductor wherein the space g4 between the first and second microstriplines 21 and 22 disposed adjacently with the same number of turns is set narrower than the space d4 between the adjacent turns of the pair of first and second microstriplines 21 and 22. (See figure 4 and column 1 lines 9-35)

One of ordinary skill in the art would have found to obvious to provide the delay of Talisa et al with the spacing between the conductor as taught by Sasaki et al.

The motivation for this modification would have been to provide a 90 degree phase shift between the input and output.

Claims 7 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Talisa et al US Patent 5,974,335 in view of Fleischer et al US Patent 4,783,359.

The primary reference, Talisa et al teaches a delay line comprising a tapered delay line (68a 68b 68c 68d), a dielectric substrate 54 and a ground plane 66. The patterned delay line has a predefined length and a predefined line width from transformer 26 to transformer 27. Figure 1a show each transformer, each having a tapered line width having a wide portion W, matching that of the deposited delay line and which tapers down to a narrow portion N, which is connected to a signal input or output. Input 15 and output 20 of each spiral line segment can be provided with coplanar line transition input and output pad pairs 22a, 22b and 24a, 24b, respectively. (Figures 1, 1a, 2 and 3)

Thus, Talisa et al is shown to teach all the limitation of the claim with the exception of the substrate comprising a flexible material.

Fleischer et al teaches a delay line disposed on a flexible substrate, which allows the delay line to rolled and placed in housing. (Figures 3, 5a 5b 5c 6a 6b)

One of ordinary skill in the art would have found to obvious to provide the delay line of Talisa et al on the a flexible substrate as taught by Fleischer et al.

The motivation for this modification would have been reduce the size of the delay circuit.

Claims 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Talisa et al US patent 5,974,335 in view of Sasaki et al US patent 6,346,863 in view of Fleischer et al US Patent 4,783,359.

The primary reference, Talisa et al teaches a delay line comprising a tapered delay line (68a 68b 68c 68d), a dielectric substrate 54 and a ground plane 66. The patterned delay line has a predefined length and a predefined line width from transformer 26 to transformer 27. Figure 1a show each transformer, each having a tapered line width having a wide portion W, matching that of the deposited delay line and which tapers down to a narrow portion N, which is connected to a signal input or output. Input 15 and output 20 of each spiral line segment can be provided with coplanar line transition input and output pad pairs 22a, 22b and 24a, 24b, respectively. (Figures 1, 1a, 2 and 3)

Sasaki et al teaches a circuit comprising a signal layer (microstriplines 21 and 22) including at least one signal conductor wherein the space g4 between the first and second microstriplines 21 and 22 disposed adjacently with the same number of turns is set narrower than

the space d4 between the adjacent turns of the pair of first and second microstriplines 21 and 22. (See figure 4 and column 1 lines 9-35)

Thus, Talisa et al and Sasaki et al are shown to teach all the limitation of the claim with the exception of the substrate comprising a flexible material.

Fleischer et al teaches a delay line disposed on a flexible substrate, which allows the delay line to rolled and placed in housing. (Figures 3, 5a 5b 5c 6a 6b)

One of ordinary skill in the art would have found to obvious to provide the delay line of Talisa et al on the a flexible substrate as taught by Fleischer et al.
The motivation for this modification would have been reduce the size of the delay circuit.

Claims 5 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Talisa et al US Patent 5,974,335 in view of Nakamura et al US Patent 5,365,203.

The primary reference, Talisa et al teaches a delay line comprising a tapered delay line (68a 68b 68c 68d), a dielectric substrate 54 and a ground plane 66. The patterned delay line has a predefined length and a predefined line width from transformer 26 to transformer 27. Figure 1a show each transformer, each having a tapered line width having a wide portion W, matching that of the deposited delay line and which tapers down to a narrow portion N, which is connected to a signal input or output. Input 15 and output 20 of each spiral line segment can be provided with coplanar line transition input and output pad pairs 22a, 22b and 24a, 24b, respectively. (Figures 1, 1a, 2 and 3) .

Thus, Talisa et al is shown to teach all the limitation of the claim with the exception a plurality of apertures extending through the substrate and placed about the signal layer and aligned to couple the signal line to the ground plane.

Nakamura et al teach a delay line with a plurality of through holes 27 and 28. (Figure 2)

One of ordinary skill in the art would have found to obvious to provide the delay line circuit of Talisa et al with the plurality of through holes as taught by Nakamura et al.

The motivation for this modification would have been to provide an alternate terminals means.

Response to Arguments

Applicant's arguments with respect to claims have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kimberly E Glenn whose telephone number is (571) 272-1761. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on (703) 308-4909. The fax phone number for the organization where this application or proceeding is assigned is (703) 308-7724.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Kimberly E Glenn
Examiner
Art Unit 2817

keg

Robert Pascal
Supervisory Patent Examiner
Technology Center 2800